REMARKS

Claims 1-31 and 96 are currently pending in the application.

35 U.S.C. § 103 Rejections:

Claims 1, 3, 6-10, 12, 15-19, 21, 28-31 and 96 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stancil, U.S. Patent 7,149,927, in view of Luke, U.S. Patent 6,505,267. Claims 4, 4, 5, 11, 13, 14, 20, and 22-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stancil in view of Luke an in further view of Applicant's Admitted Prior Art (AAPA). Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, fail to teach or suggest all of the elements of the independent claims. The teachings of Luke were presented in prior office action responses. Stancil teaches "[an] emulator [] provided on an electronic assembly that permits external logic to communicate with test logic on the electronic assembly over an electrical interface that has fewer signals than the electrical interface associated with the test logic itself. In this way, external logic can communicate with test logic on the electronic assembly over an interface that uses fewer signal lines thereby permitting the electronic assembly's electrical connector to be smaller than it otherwise would be. In accordance with one embodiment, the test logic's interface comprises a JTAG interface having four signals (with an optional fifth signal) and the interface between the emulator and the external logic comprises a two wire SMBus communication link. In fact, the SMBus interface may already be provided to the electronic assembly for other reasons such as to provide control to and obtain status information from another component on said electronic assembly." (Abstract, Stancil).

Independent claim 1 recites, in pertinent part:

"An SMBus host controller comprising

a memory storing microcode comprising at least two programs each for handling a bus command protocol, each program comprising at least one instruction; ...
a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory; ... and
an address register array comprising a plurality of starting addresses of programs stored in said memory, said register comprising an offset for pointing at a specific register in said address register array (Emphasis added).

Independent claims 10 and 19 recite similar combinations of features.

Neither Stancil nor Luke, taken singly or in combination, teach or suggest these combinations of features, including those highlighted above. In the office action, the Examiner contends that Luke and Stancil, taken in combination together, teach an SMBus handler comprising an address register array having a plurality of starting addresses of programs stored in the recited memory, and wherein the register comprises an offset for pointing at a specific register in the address register array. In support of this contention, the Examiner cites Luke at col. 4, lines 31-42, which states the following:

Access to the sequencer ram 40 is dependent on the activity of the sequencer 46. If the sequencer 46 is active, access to the sequencer ram 40 is locked out to other circuitry in the USB bridge 16. In the case of descriptor data, the USB interface 42 clears the sequencer ram 40 and signals the ROM/EEPROM interface 36 to retrieve **data** starting at a specified address. The USB interface 42 then begins passing data back to

> the USB core 30 when the sequencer ram 40 has data available. Device ID data for peripheral device 20 is retrieved in much the same manner as descriptor data, except that the parallel port 44 is directed to retrieve the data rather than the ROM interface 36. (Emphasis added).

Nothing in the above citation teaches or suggests, "an address register array comprising a plurality of starting addresses of **programs**" as recited in claim 1 and similarly recited in other ones of the independent claims. The above citation of Luke appears to teach retrieving descriptor data from a specified address, but makes no mention of "a plurality of starting addresses of programs" or a register array storing these starting addresses. Furthermore, the above citation provides no teaching or suggestion of a "register comprising an offset for pointing at a specific register in said address register array," or any mention of an offset for pointing at a specific register in an address register array. Furthermore, these limitations are not disclosed elsewhere in Luke. Stancil provides no teaching or suggestion that, taken singly or in combination with Luke, results in these limitations. Accordingly, Stancil in view of Luke fails to teach or suggest "an address register array comprising a plurality of starting addresses of programs stored in said memory, said register comprising an offset for pointing at a specific register in said address register array."

Stancil in view of Luke further fails to teach or suggest "a finite-state machine configured to ... manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory" as recited in claim 1 and similarly recited in the other independent claims. In the office action, the Examiner refers to state machines 112 and 116 disclosed by Stancil (in Fig. 2) as reading on Applicant's recited finite state machine. The Examiner further refers to Stancil at col. 4, lines 20-32. Col. 4, lines 14-32 of Stancil state the following:

> FIGS. 2-5 provide further detail regarding SMBus-to-JTAG emulator 110 pertaining to how the emulator converts between SMBus and JTAG. A more detailed block diagram of emulator 110 is shown in FIG. 2. As

shown therein, the emulator 110 preferably comprises an SMBUs state machine 112, an SMBus packet decoder/encoder 114 and a JTAG interface logic state machine 116. The SMBus state machine 112 comprises logic that receives SMBus packets from the host test system 102 and, with the help of the SMBus packet decoder/encoder 114, extracts the information from the packets necessary for the JTAG logic 122. The decoder/encoder 114 then creates JTAG-compliant communications that are sent to the JTAG logic 122 associated with the DUT 120 under the control of the JTAG interface logic state machine 116. Similarly, JTAG communications from the JTAG logic 122 are received by state machine 116, decoded by decoder/encoder 114 and are converted to SMBus-compliant packets by decoder/encoder 114 and provided to the host test system 102 under the control of the SMBus state machine 112. (Emphasis added).

Nothing in the above citation teaches or suggests that either of the state machines disclosed by Stancil "manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory" as recited in the independent claims. Applicant reminds the Examiner that MPEP 2143.03 states: ""All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." The disclosure of state machines in Stancil is not sufficient to show that all of the limitations of Applicant's recited state machine are taught or suggested therein. Furthermore, Luke provides no additional teaching or suggestion, taken singly or together with Stancil, which would result in a state machine as recited in the independent claims. Accordingly, Stancil in view of Luke fails to teach or suggest "a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory"

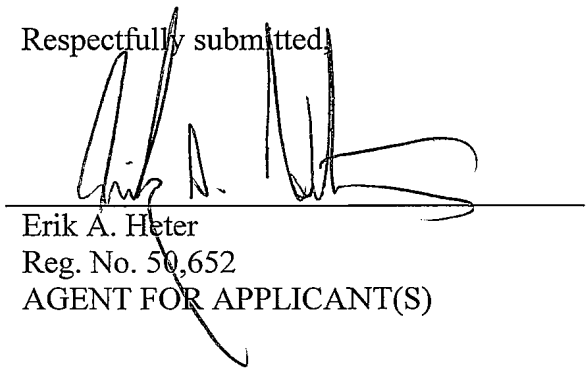
For at least the reasons given above, Applicant submits that Stancil in view of Luke fails to teach or suggest all of the elements of the independent claims. Accordingly, removal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-92201/EAH.

Respectfully submitted,



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